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**BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES**



Application Number: 09/944,230
Filing Date: August 30, 2001
Appellant(s): WHITMAN ET AL.

Thomas L. Dickey
For Appellant

**EXAMINER'S ANSWER**

This is in response to the appeal brief filed 04/04/2005 appealing from the Office action mailed 11/03/2004.

**(1) Real Party in Interest**

A statement identifying by name the real party in interest is contained in the brief.

**(2) Related Appeals and Interferences**

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

**(3) Status of Claims**

The statement of the status of claims contained in the brief is correct.

**(4) Status of Amendments After Final**

No amendment after final has been filed.

**(5) Summary of Claimed Subject Matter**

The summary of claimed subject matter contained in the brief is deficient. 37 CFR 41.37(c)(1)(v) requires the summary of claimed subject matter to include: (1) a concise explanation of the subject matter defined in each of the independent claims involved in the appeal, referring to the specification by page and line number, and to the drawing, if any, by reference characters and (2) for each independent claim involved in the appeal and for each dependent claim argued separately, every means plus function and step plus function as permitted by 35 U.S.C. 112, sixth paragraph, must be identified and the structure, material, or acts described in the specification as corresponding to each claimed function must be set forth with reference to the specification by page and line number, and to the drawing, if any, by reference characters. The brief is deficient because it fails to supply a concise explanation of the subject matter defined in claims 1 and 15 (the independent claims involved in the appeal),

referring to the specification by page and line number, and to the drawing, if any, by reference characters.

**(6) Grounds of Rejection to be Reviewed on Appeal**

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

**(7) Claims Appendix**

The copy of the appealed claims contained in the Appendix to the brief is correct.

**(8) Evidence Relied Upon**

The following is a listing of the evidence (e.g., patents, publications, Official Notice, and admitted prior art) relied upon in the rejection of claims under appeal.

US 6,358,793 A (YATES et al) 19 March 2002, figures 11, 12, 17, column 6 line 50 and column 10 lines 1-31.

US 6,278,153 A (KIKUCHI et al) 21 August 2001, figures 6B-6F and column 19 lines 35-67 and column 20 lines 13-27.

US 6,461,932 A (WANG) 08 October 2002, figure 4F and column 6 lines 23-51 and column 8 lines 26-39.

US 5,663,090 A (DENNISON et al.) 02 September 1997, figure 4b.

**(9) Grounds of Rejection**

The following ground(s) of rejection are applicable to the appealed claims:

Claims 15-20, 23, and 24 stand rejected under 35 U.S.C. 102(e) as being anticipated by YATES et al. (6,358,793).

With regard to Claims 15,17-20, 23, and 24 Yates et al. discloses a semiconductor device structure with a substantially planar surface, comprising a substrate (5,10) including at least one recess 20 formed therein, and a material layer 90 disposed at least partially over the substrate (5,10) and at least one intermediate layer 30 that comprises a conductive material (conductive

HSG silicon, note column 6 line 50), between the substrate (5,10) and the material layer 90, so that the material layer 90 and the at least one intermediate layer 30 (specifically that part of layer 30 lying inside recess 20) each at least partially fill the at least one recess 20, wherein the surface of the material layer 90 is a substantially planar surface, is free of abrasive planarization-induced defects, and is substantially free of hills and valleys; and where at least one region of the at least one intermediate layer 30 and at least one region of the substrate (5,10) is exposed through the material layer 90, and the material layer 90 has a thickness that is less than a depth of the at least one recess 20. Note figures 11, 12, 17, column 6 line 50 and column 10 lines 1-31 of Yates et al.

With regard to Claims 15 and 16 Yates et al. discloses a semiconductor device structure with a substantially planar surface, comprising a substrate (5,10,30) including at least one recess 20 formed therein, and a material layer 90 disposed at least partially over the substrate (5,10,30) so that the material layer 90 at least partially fills the at least one recess 20 and is substantially free of hills and valleys; and where at least one region (30) of the substrate (5,10,30) is exposed through the material layer 90. Note figures 11, 12, 17, column 6 line 50 and column 10 lines 1-31 of Yates et al.

Claims 1,3, 11-13, 21, and 22 stand rejected under 35 U.S.C. 102(e) as being anticipated by KIKUCHI ET AL. (6,278,153).

Kikuchi et al. discloses a semiconductor device structure with a substrate (21,23) including at least one recess 23A formed therein, and a material layer 20 disposed over the substrate (21,23) and substantially filling the at least one recess 23A, wherein the surface of the material layer 20 is a substantially planar surface, is free of abrasive planarization-induced defects, and is substantially free of hills and valleys; and wherein the substrate (21,23) comprises

a stacked capacitor structure (22,24,25,26) and the at least one recess 23A comprises at least one container (formed by layer 27) recessed in an insulator layer 23 of the stacked capacitor structure (22,24,25,26). Note figures 6B-6F and column 19 lines 35-67 and column 20 lines 13-27 of Kikuchi et al.

With special regard to claims 3,12, and 13, Kikuchi et al. discloses that the material layer 20 comprises a mask material (note column 20 lines 14-17), the mask material substantially filling the at least one container (formed by layer 27), wherein the mask material has a thickness of (note the thickness disclosed by figure 6F) less than a depth of the at least one container (formed by layer 27).

Claims 1,21,22, 15,16,23, and 24 stand rejected under 35 U.S.C. 102(e) as being anticipated by WANG (6,461,932), cited by the applicant on 11/03/03.

Wang discloses a semiconductor device structure with a substantially planar surface, comprising a substrate 40 including at least one recess 54 formed therein; and a material layer 56A disposed over said substrate 40 and substantially filling said at least one recess 54, so as to at least partially fill said at least one recess 54, wherein at least one region of said substrate 40 is exposed through said material layer 56A, and wherein the surface of said material layer 56A is a substantially planar surface, is free of abrasive planarization-induced defects, and is substantially free of hills and valleys. Note figure 4F and column 6 lines 23-51 and column 8 lines 26-39 of Wang.

Additionally, although Applicant does not argue the correctness of the rejection, claim 4 stands rejected under 35 U.S.C. 103(a) as being unpatentable over KIKUCHI et al. (6,278,153) in view of DENNISON et al. (5,663,090).

Kikuchi et al. discloses a semiconductor device structure with all the limitations of claim 4 except that the substrate include at least one conductively doped region continuous with a surface of the semiconductor substrate and adjacent the at least one recess. Note figure 6F of Kikuchi et al.

However, Dennison et al. discloses a semiconductor device structure with substrate 40 including at least one conductively doped region 41 that is adjacent to a recess (the recess being filled with lower electrode 43 of a stacked capacitor structure. Note figure 4b of Dennison et al. Therefore, it would have been obvious to a person having skill in the art to replace the substrate of Kikuchi et al.'s semiconductor device structure with the substrate including at least one conductively doped region that is adjacent a recess containing a stacked capacitor structure, such as taught by Dennison et al. in order to utilize the semiconductor device structure of Kikuchi et al. alongside a MOSFET such as taught by Dennison et al. to thus utilize the semiconductor device structure of Kikuchi et al. as the capacitor of a DRAM memory.

Applicant has argued that claim 4 is allowable because claim 1, from which claim 4 depends, is allowable. See page 15 of the Brief.

**(10) Response to Argument**

Recently, in *Playtex Products Inc. v. Procter & Gamble Co*, the Federal Circuit stated:

> "The term 'substantial' is a meaningful modifier implying 'approximate,' rather than 'perfect.'" Liquid Dynamics, 355 F.3d at 1368. But the definition of "substantially flattened surfaces" adopted by the district court introduces a numerical tolerance to the flatness of the gripping area surfaces of the claimed applicator. That reading contradicts the recent precedent of this court, interpreting such terms of degree. In Cordis Corp. v. Medtronic AVE, Inc., 339 F.3d 1352, 1361 [67 USPQ2d 1876] (Fed. Cir. 2003), we refused to impose a precise numeric constraint on the term "substantially uniform thickness," noting that the proper interpretation of this term was "of largely or approximately uniform thickness" unless something in the prosecution history imposed the "clear and unmistakable disclaimer" needed for narrowing beyond this plain-language interpretation. Id. Moreover, in Anchor Wall Sys. v. Rockwood Retaining Walls, Inc., 340 F.3d 1298 [67 USPQ2d 1865] (Fed. Cir. 2003), we held that "the phrase 'generally parallel' envisions some amount of deviation from exactly parallel," and that "words of approximation, such as 'generally' and 'substantially,' are descriptive terms 'commonly used in patent claims to avoid a strict numerical boundary to the specified parameter.'" Id. at 1311. In

> support of this holding, we noted that "nothing in the prosecution history [of the Anchor Wall patent]. clearly limit[ed] the scope of 'generally parallel' such that the adverb 'generally' does not broaden the meaning of parallel." Id. Similarly, in this case we find that in claiming, "substantially flattened surfaces," Playtex claimed more than flat surfaces.

*Playtex Products Inc. v. Procter & Gamble Co.*, 73 USPQ2d 2010, 2015 (Fed.Cir 3/7/2005). The examiner believes that, in claiming "a surface substantially free of hills and valleys," in independent claims 1 and 15, Applicant has claimed a variety of surfaces, more than Applicant would have claimed had Applicant chosen to claim, within numerical or parametric limits, the degree to which his surface is free from hills and valleys.

It is argued, at page 10 of Applicant's Brief, that "Wang notes, at column 6, lines 32-34, that 'slight depressions in upper smoothening surface 62 at the locations of the deepest parts of the depressed portion of upper dielectric surface 58.'" However, Wang also says, column 6 line 31-32, that "Ideally, upper smoothening surface 62 is largely planar." Wang goes on to say, lines 34-37, that "Compared to upper dielectric surface 58, upper smoothening surface 62 is largely planar." The examiner believes that the modifiers "largely," "approximately," "generally," and "substantially," are all roughly equivalent, and that a "planar" surface is free of hills and valleys.

It is argued, at page 11 of Applicant's Brief, that "While Yates's figures depict an edge of an upper surface of the photoresist layer 40, at the depicted cross-section of the semiconductor device structure, as being substantially linear, the description of Yates is silent as to whether or not the upper surface of the photoresist layer 40 is actually substantially free of hills and valleys, as recited in independent claim 15." However, Yates clearly knows how to draw a surface that, in fact, has hills and valleys. Look at the surface of part 30 in Yates's figure 2, or the surface of part 220 in Yates's figure 7. By implication, surfaces Yates draws differently from the bumpy

surfaces of parts 30 and 220 are flat surfaces. Compared to these surfaces, the upper surface of photoresist layer 40 in Yates's figures 11, 12, 17 is indisputably flat.

It is argued, at page 12 of Applicant's Brief, that "Claim 20 is further allowable since Yates neither expressly nor inherently describes a material layer (i.e., either the photoresist layer or the resulting mask layer thereof that has a thickness which is less than the depths of the containers thereof. The relative dimensions shown in the drawings of Yates cannot be relied upon since Yates does not disclose that the drawings are to scale and is silent as to dimensions." M.P.E.P. 2125." However, in Yates's figure 4, material layer 90 has a thickness 130 that is clearly less than the depth of container 20. This is because the drawing depicts thickness 130 as being smaller than the depth.

It is argued, at page 13 of Applicant's Brief, that "[it is] submitted that, in view of the guidance provided by M.P.E.P. 2125, reliance upon the drawings of Kikuchi is improper, since the specification does not indicate that the features (e.g., straight lines) of the simplified drawings are to be taken at face value." Applicant does not cite authority for his view that everything in the drawings must be viewed with dark suspicion. The examiner believes to the contrary, that even a design patent (which has no written description) may fully disclose an invention. See *Vas-Cath Inc. v. Mahurkar* 19 USPQ2d 1111 (Fed. Cir. 1991). The question, regardless of whether the prior disclosure is written or drawn, is whether the patent's disclosure allows "one skilled in the art to visualize or recognize the identity of the subject matter purportedly described." *Enzo Biochem, Inc. v. Gen-Probe Inc.*, 323 F.3d 956, 968; 63 USPQ2d 1609, 1616 (Fed. Cir. 2002), citing *Regents of Univ. of Cal. v. Eli Lilly & Co.*, 119 F.3d 1559, 1573, 43 USPQ2d 1398, 1406 (Fed. Cir. 1997).

In the case at hand what one skilled in the art would have had to visualize or recognize in Kikuchi, to anticipate claims 1 and 15, would have been "a surface substantially free of hills and valleys." The question is whether, in looking at Kikuchi's figures 6B and 6F and reading the accompanying description at column 19 lines 35-67 and column 20 lines 13-27, one skilled in the art would visualize or recognize such a surface. Granted, there is nothing in the drawings but a flat, horizontal line. However, those skilled in the semiconductor art have become accustomed to visualizing flat surfaces upon apprehending such a drawing.

**(11) Related Proceeding(s) Appendix**

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

**(12) Conclusion**

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

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